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Gate all around MOSFET

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Abstract
Introducing a new route for transistor scaling, the cylindrical gate all around (GAA) MOSFET is a radical idea and a prospective contender to replace conventional MOSFETs. An investigation of the electrical properties of cylindrical GGA (CGAA) MOSFETs with 50nm channel length (Lg) and 10nm channel thickness (tsi) is carried out in this study. Calculations and analyses of different electrical properties such as the on current (ION) and subthreshold leakage current (IOFF) at various device design parameters, as well as the threshold voltage (Vth) and DIBL, are performed. All of the Cylindrical GAA MOSFETs' device performance is studied using the Silva Atlas device simulator.

Keywords: Cylindrical gate all around (GAA) MOSFET, subthreshold leakage current (I_{OFF})

Introduction
Electronics companies have been paying attention to the rapid growth of CMOS technology in recent decades. In order to achieve greater density, increase the performance of SOI chips, and reduce the cost of electronic products, scaling is a must. A trade-off occurs with increasing numerous defects, such as drain-induced barriers, hot carrier effects and so on.
As a result of these faults, also known as short channel effects, it is impossible to achieve the projected performance gains [1-2].
It is imperative that new circuits and design methodologies be used to take advantage of the latest technology in order to address these shortcomings.
Multi-gate silicon on insulator (SOI) technology has been offered as an alternative to the MOSFET [3]. New technologies, such as the CGAA MOSFET (circular gate all around), allow for even greater scalability without compromising device performance [4, 5]. Cylindrical GAA MOSFETs have a better packing density than conventional multiple-gate MOSFETs because of their higher driving current and shorter length.
A further advantage of CGAA MOSFETs over other multi-gate designs is their good electrostatic channel management, lack of floating body effect, robustness against SCEs, greater scaling possibilities, and optimum sub-threshold swing [6]. As a result, CGAA MOSFETs are an excellent choice for CMOS devices at the nanoscale [7].
Threshold voltage (Vth) and on-off ratio (ION/IOFF) are two other essential device characteristics that are highly dependent on the geometry of the device, such as channel length (Lg) and channel thickness (IOFF) (tsi). Electrical characteristics such as threshold voltage (Vth) and drain current are reported in this study analytically.

Structure and specification of the device
Cylindrical GAA (CGAA) MOSFET structures employed in simulation are schematically shown in Figure 1, as illustrated. The Atlas Silvaco tool is used to create this structure. The radial and lateral directions are considered to be along the cylinder's radius and z-axis, respectively, as seen in Figure 1.

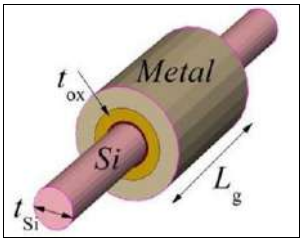


Fig 1: Schematic Structure of Cylindrical Gate All Around (GAA) MOSFET

Table 1 shows the specifics of the device physical characteristics that were used in the design. GAA MOSFETs with n-type channels need an SOI substrate. Assuming a work function of 4.44 eV (Lg), the length of the gate (Lg) is 30nm. In this case, the diameter of the tsi is 10 nanometers. One nm thick gate oxide (tox) of SiO2 is used in the fabrication of our transistors.

Table 1: Device Dimensions & Dopings

Parameter	Value
Gate Length (Lg)	30nm
Radius ($t_{si}/2$)	5nm
OxideThickness (t_{ox})	1nm
Channel Doping	$1.0x10^{18}$ cm^{-3}
Source Doping (N_D)	$1.0x10^{20}$ cm^{-3}
Drain Doping (N_D)	$1.0x10^{20}$ cm^{-3}

The peak concentration of 1.0x1020 cm-3 was used for the source/drain extension doping profile.

A cylindrical GAA MOSFET with a channel length of 30 nm was employed in the simulations shown in Figure 2.

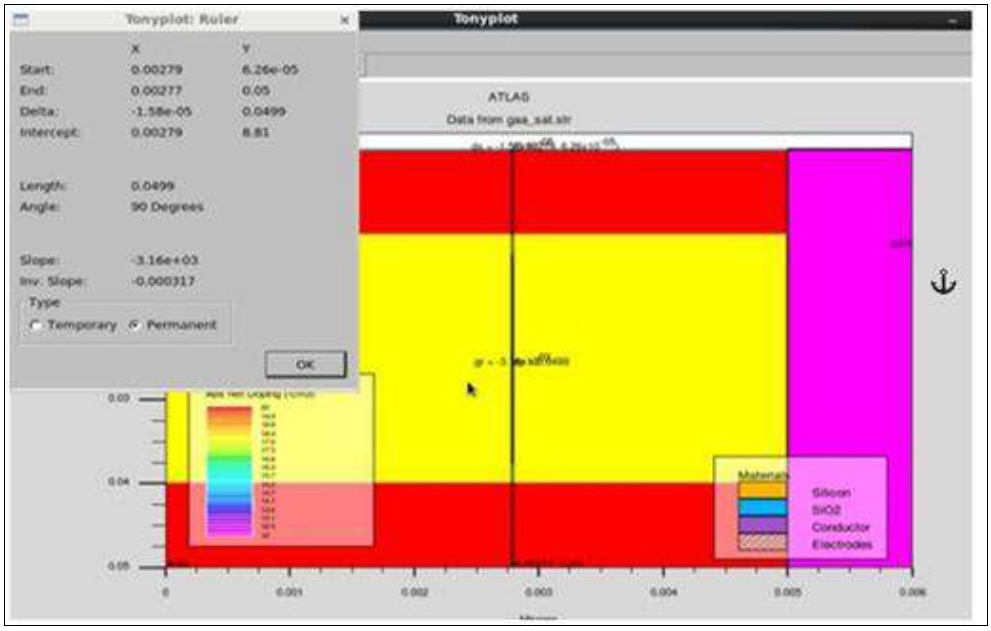


Fig 2: Cross sectional view of GAA structure for channel length (Lg)

A cross sectional picture of the GAA structure with a silicon thickness of radius (tsi/2) 5nm and an oxide thickness of 1nm was employed in the simulation.

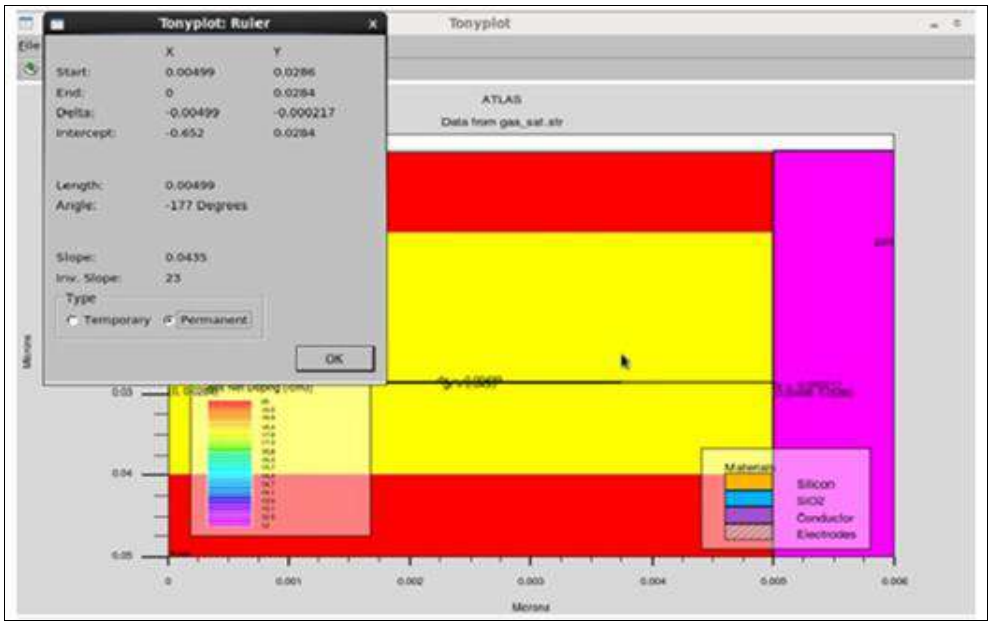


Fig 3: Oxide (TOX) and silicon (silicone) thicknesses

Oxide (TOX) and silicon (silicone) thicknesses are shown in Fig 3 as cross sections of GAA structure (TSI). To prevent a sudden transition, a uniform donor (ND) doping profile plot between the source and drain with fixed charges 1x1020 cm-3 was utilised in the simulation (Fig 4). Metal gate work function M=4.4eV has been examined.

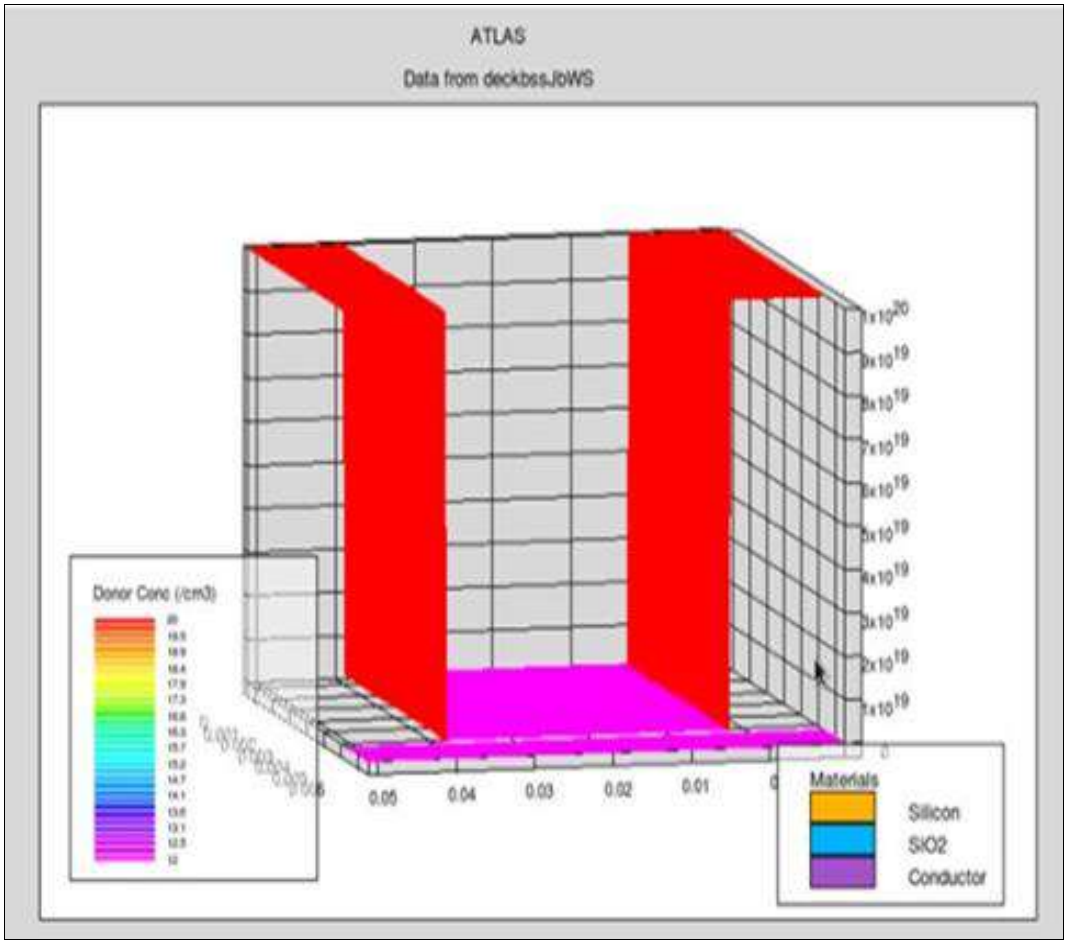


Fig 4: Donor Concentration Graph

Literature survey

The future generation devices demand small size transistors. As the size of traditional MOSFETs is scaled down, the performance of device diminishes due to the occurrence of short-channel-effects (SCEs) [16]. Multigate MOSFETs have paved the way to enhance the performance in nano-scale regime. The ITRS espy the usefulness of these multigate MOSFETs and name them as "Advanced Devices". The reduction in device dimensions causes the close proximity between the source and drain which diminutive the capacity of the gate electrode to control the channel. The presence of short channel effects at scaled devices squeezes the MOSFETs [3]. The researchers are trying to find out a device which has small size and negligible presence of short channel effects. The multigate MOSFET is the most promising device which shows higher performance. This structure includes double-gate (DG), triple-gate (TG) and gate-all-around (GAA) MOSFET which amends performance in comparison to traditional single gate MOSFETs. In double gate MOSFETs, two gates are present to control the channel current. But SCEs are still present in this device. To avoid the SCEs, device should be fully surrounded by the gate material and device is known as gate-all-around (GAA) MOSFET. At smaller channel lengths, it is a huge task to reduce the leakage currents. The gate and channel engineering techniques are used to further boost up the device efficiency. Gate engineering was introduced by Long *et al*. and it produced a dual material gate MOSFETs (DMG). This device has two different metals at the gate with distinct work functions that produce step potential profile which suppresses 33 the SCEs as compared to a single gate MOSFET. Reddy & Kumar have developed an analytical model for dual material double gate MOSFET. This structure incorporates the benefits of both DMG and DG MOSFETs. The amend trans conductance and electric field near to drain side decreases reportedly by the DM-DG structure. The main disadvantage of DM-DG structure is that threshold voltage vigorously depends upon the thickness of silicon film. Kumar *et al*. carried out the performance analysis of MOSFET (DM-SG). It is found out that the performance of DMSG is better than DMDG structures. In order to further reduce the SCEs, a new device is proposed in which gate electrode consist of three different metals with distinct work function known as triple material surrounding gate MOSFETs (TMSG) [15], In conventional MOSFET, the value of electric field is very low near the source side and approaches a high value at the drain end. This is mainly due to the injection of hot electrons between gate and drain and reduces the performance and lifetime of the device. The value of electric field near the drain side should be decreased to a lower value to reduce the leakage current without reduction in Ion values. The halo implant MOSFET reduces the hot carrier effect (HCEs), gate stack (GS) reduces the gate leakage current and gate engineering

such as dual-material (DM) and tri-material (TM) structures reduce the SCEs [13].

Experiments

Figure 5 depicts a 3D and 4D III-V transistor with a 12 or 32 NW array in a 3D transistor. As shown in Table 1 of this research, the NW array, NW size, EOT and indium composition of the InGaAs channels are all broken out in detail. Al2O3 (EOT=2.2nm) and In0.65Ga0.35As inclusion in the NWs of the III-V 3D transistors studied in Sample 1 improve gate electrostatic control and channel mobility, respectively. In Ref. [1], a manufacturing method for III-V 3D transistors was devised. atomic layer deposition was used to deposit the Al2O3/WN high-k/metal gate stack (ALD). In 5nm increments, the nanowire width (WNW) is increased from 25nm to 35nm. Sample.

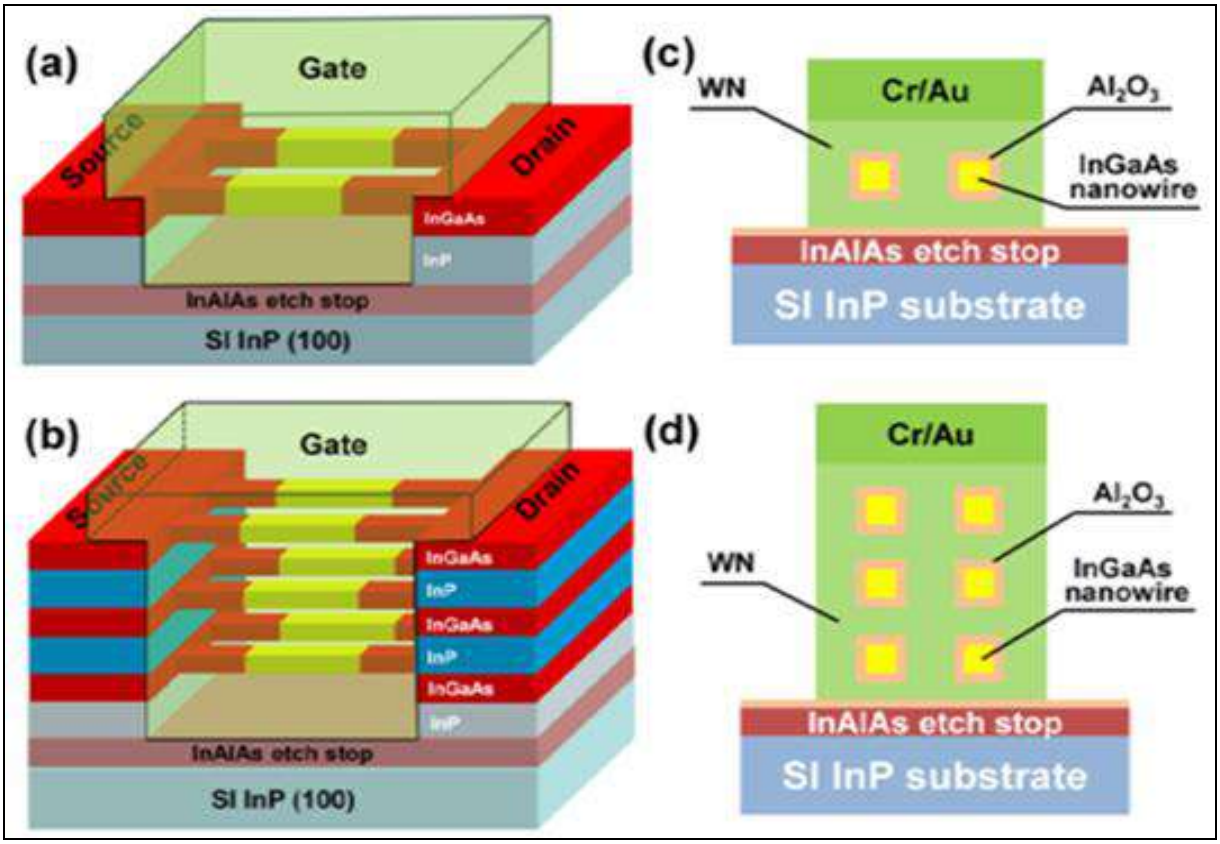


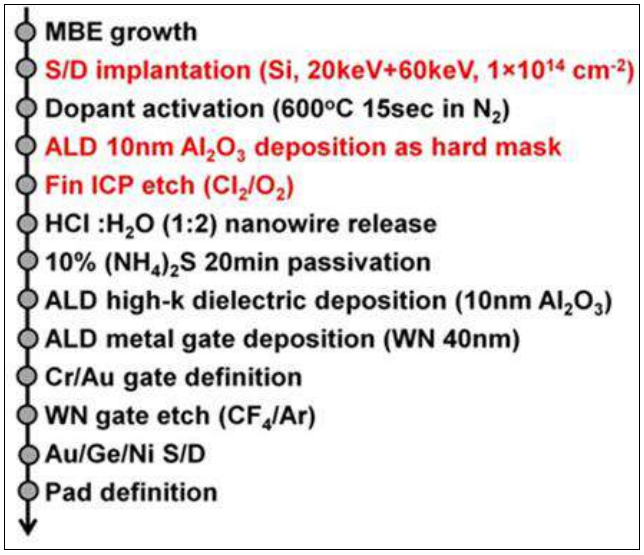
Fig 5: (a) 3D and (b) 4D III-V transistor schematics are shown in

Fig 5: The cross-sectional views of the NWs in (a) and (b) are shown in (c) and (d), respectively, and exhibit 12 and 32 NW arrays

	Structure	Nanowire Array (H×W)	Al_2O_3 Thickness (nm)	W_{NW} (nm)	H_{NW} (nm)	$In_xGa_{1-x}As$ (x)
Sample 1 (This work)	3D	1×4	5	25 30 35	30	65%
Sample 2 (This work)	4D	3×2 3×4	10	20 (Layer1) 60 (Layer2) 100 (Layer3)	30	53%
Sample 3 (IEDM11)	3D	1×1 1×4 1×9 1×19	10	30 50	30	53%

Fig 6: Table 1 NW array (vertical-lateral), NW size and EOT splits for Samples 1 and 2 manufactured in our study, and Sample 3 in Ref. [1].

For the first time, 3D transistors using 10nm Al2O3 (EOT=4.5nm) and 3x2 or 3x4 NW arrays have been shown. The process flow for III-V 4D transistors is shown in Figure 2. In addition to the ones described in [1], new process technologies are shown in red. There are three layers of InGaAs NWs stacked vertically in the production process of III-V 4D transistors.



For the III-V 4D transistors with vertical and lateral integration of InGaAs NWs, see Fig. 2 for the fabrication process flow. The red highlighting indicates newly developed process technologies in addition to those in Ref. [1].

Semi-insulating InP (100) substrates were used to begin production of III-V 4D transistors. After a 100nm InAlAs etch stop layer and an 80nm undoped InP sacrificial layer were deposited on the InP substrate, three layers of 30nm In0.53Ga0.47As channel were developed, each with a 40nm InP layer sandwiched between each channel layer (Fig. 3-1). Each of the three vertically stacked channel layers was doped with a dosage of 11014 cm-2 in a two-step Si implantation at energies of 20keV and 60keV. A hard mask of 10nm ALD Al2O3 was produced and designed to replace the electron beam resist [1], resulting in good etching selectivity and removing resist redeposition. A new Cl2/O2 fin etching process was developed to increase the etch rate and improve the sidewall quality, replacing the BCl3 based etching [1]. (Fig. 3-5). The NW arrays designed in the [100] direction were released using an HCl-based solution (Fig. 3-6). The selective wet etching process may be better controlled with the help of the InAlAs etch stop layer. The sample was immediately placed into the ALD reactor for Al2O3 and WN deposition at 300 °C and 385 °C, respectively, after a 10 percent (NH4)2S passivation (Fig. 3-7). The source and drain contacts were then produced using a CF4/O2 based gate etch method, followed by electron beam evaporation of Au, Ge, and Ni and a liftoff procedure (Fig. 3-8). At 350 ^{0}C, the Cr/Au test pads were established after the alloy was formed.

An SEM picture of a III-V 4D transistor with four parallel NW stacks is shown in Fig. 4(a). Fin structure after dry etching with Cl_2/O_2 is shown in Figure 4(b). There are three layers of interest here: the Al2O3 etch mask and the InGaAs channel layers. Cross-sectional TEM pictures of InGaAs 31 and 34 NW arrays reveal that the ALD gate stack was coated around each of these devices, as shown in Fig. 4(c)-(d).

Nanowire. Layers 1, 2, and 3 have WNWs of 20, 60, and 100nm, respectively. This can only be accomplished with the improvement of an anisotropic dry etch technique. For each layer, MBE specifies that the HNW is 30nm. For the gate metal, the ALD procedure of producing highly conformal WN sheets is detailed in Ref [4]. A sample of holes with a diameter of 0.3 m and a depth of 11 m was used to test WN's outstanding step coverage (aspect ratio = 37:1). On a structure with an aspect ratio of 37, the film thickness was 41 nm in the top and bottom zones, resulting in 78 percent step coverage. The III-V 4D transistor process relies heavily on a high-quality conformal ALD WN process. A Vistec VB-6 UHR electron-beam lithography equipment was used to create all of the designs. MOSFET output characteristics were measured using a Keithley 4200.

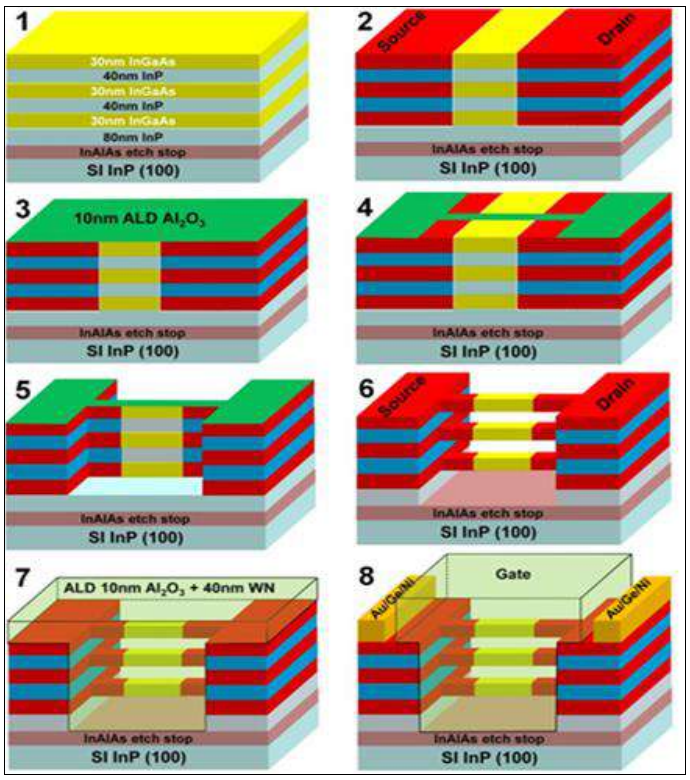


Fig 7: Schematic diagram of the key process steps in the fabrication of III-V 4D transistors with 3 lay rs of InGaAs NWs stacked vertically

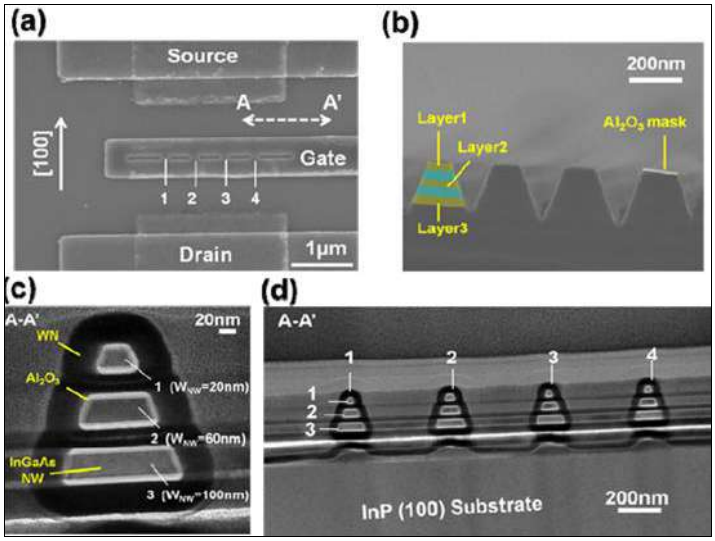


Fig 8: A top view SEM image

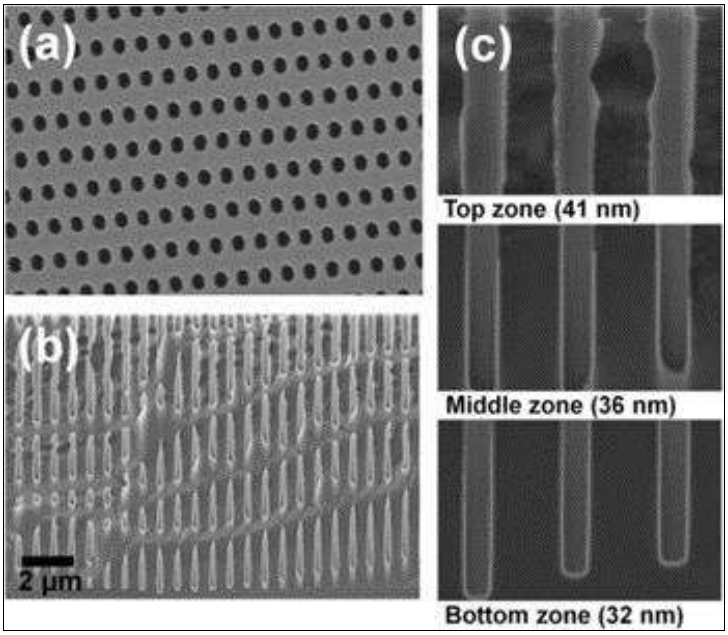


Fig 9: SEM pictures of an ALD WN coated hole sample with a 37:1 aspect ratio are shown in Figures 5(a), (b), and (c). In the top, middle, and bottom zones, film thicknesses of 41nm, 36nm, and 32nm were achieved, representing 78 percent step coverage

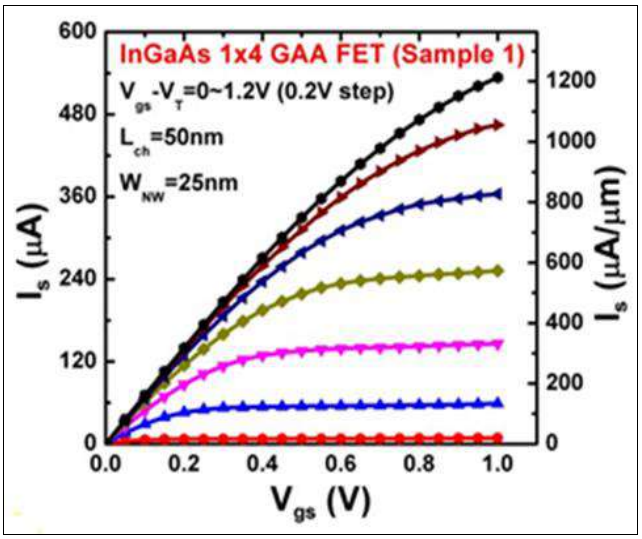


Fig 10: Output characteristics of a III-V 3D FET with 1×4 NW array (Sample 1). Current is normalized by the total perimeter of the NWs

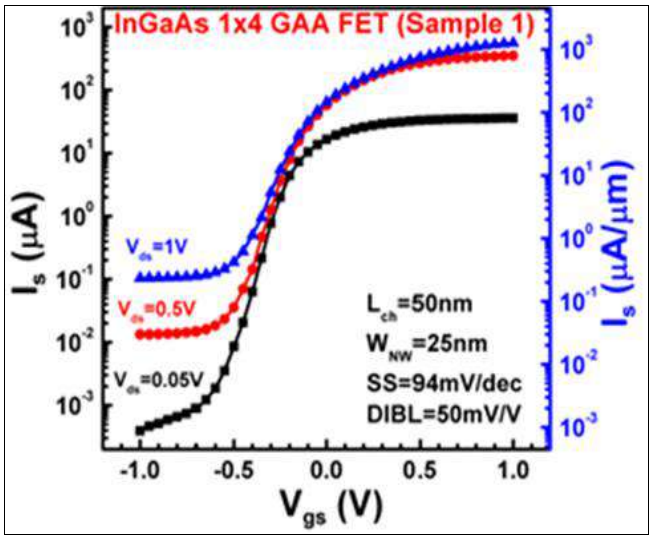


Fig 11: Transfer characteristics of a III-V 3D FET with 1×4 NW array (Sample 1)

Results and Discussion

The GAA MOSFET transfer properties are shown in Figure 12. Different drain voltages were used in the simulation.

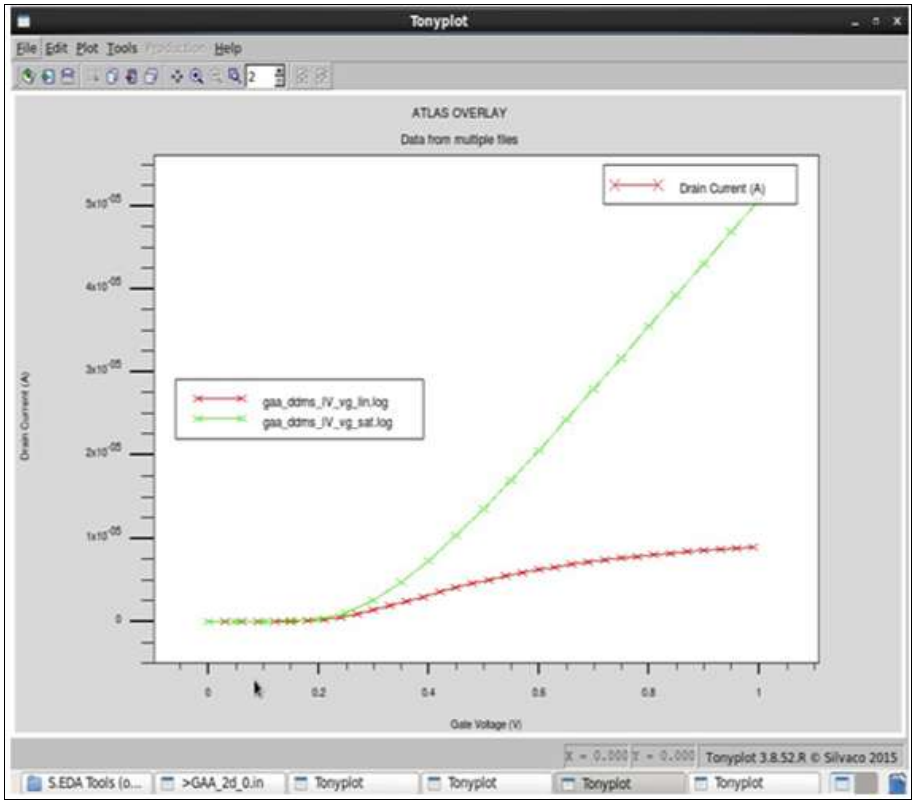


Fig 12: The GAA MOSFET transfer properties

For VDS =1 V and 0.1 V GAA, the MOSFET threshold voltage (Vth) extraction was conducted using a constant current definition that is generally applicable to measure. When simulating, we use a constant current of 1x10-7 A/m as a starting point. For different gate voltages, the GAA MOSFET's transfer characteristics are shown in Fig. 13. When the drain voltage was raised from 0.1 to 1 V, the DIBL was measured as the difference between the threshold voltages.

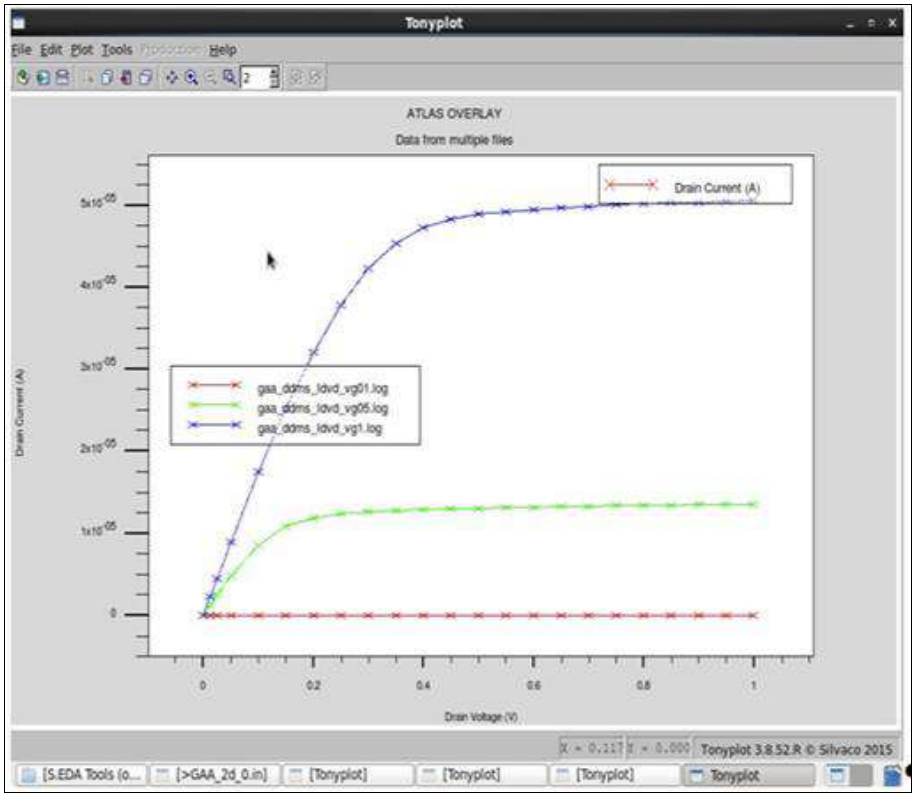


Fig 13: The GAA MOSFET's transfer characteristics

For VDS=1 V and VGS=0.1 V, Figure 6 shows the drain current (ID) as a logarithmic function of gate voltage (VGS).

The ION and IOFF driving currents were measured at different gate voltages (VGS). IOFF was acquired at VG=0.1 V and ION was obtained at VG=1.0 V in Fig 7.

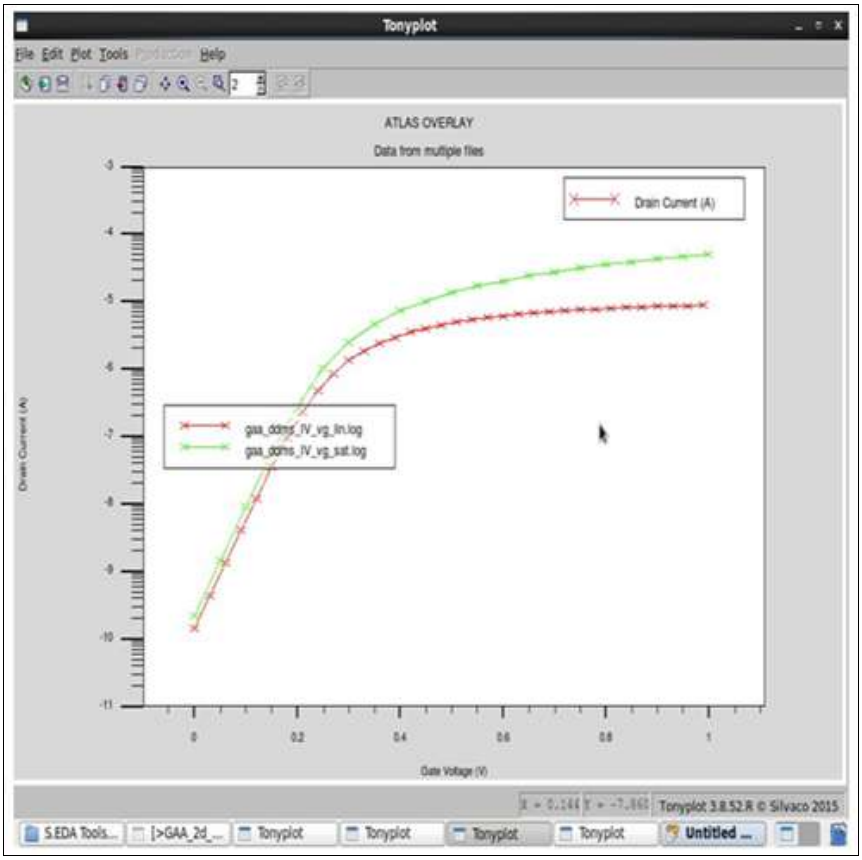


Fig 14: I_{ON} & I_{OFF} current for different Gate voltage V_{GS}

The Result of Simulation were summarised in Table 2.

Table 2: Simulated value of Electrical Characteristics of the structure

Parameter	Value
VTH	0.17 V
SS	0.06159 mV/dec
DIBL	0. 0182544 mV/V
ION	7.74e-5 A
IOFF	1.74e-10 A

Findings and research gaps

Over recent decades, continued decline over planar MOS transistors has guided a sustainable development in integrated circuit technology. The technological scaling down contributed to the multiple-faceted development of the integrated circuit (IC) system to enhance performance, speed and ULSI incorporation, etc. Nonetheless, because of severe SCE's such as DIBL, subliminal swing (SSs), velocity saturation, large drain current, etc. in ultra-small transistors, the efficiency improvement based on a steady downsizing of transistors has reached the choke point. The two- dimensioned effects (SCE and DIBL) are becoming ever more significant as the dimensions of the device reach the sub-micron dimension. Even if the continuous scaling paradigm is implemented, incremental field approximation is null and a field is changed significantly. Owing to a much slower voltage drop in actual circuitry in contrast with the criteria for constant field scaling the field still decreases. Through general scaling theory, this requirement for continuous field scaling has been presented.

Conclusion

Device reliability will be improved by using a GAA MOSFET to eliminate short channel effects (SCE). Subthreshold swing (SS), off-state current (IOFF), and dynamic on-state bias (DIBL) are all improved in GAA MOSFETs. The simulation findings show better suppression of SCEs and an increase in the device's dependability.

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