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Cylindrical gate all around MOSFET

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Abstract
Here, the electrical and physical properties of MOSFET are discussed. MOSFET architectures have been analysed according to their categories, as well as a three-dimensional schematic of the bulk MOSFET. The output I-V characteristics, the transfer characteristics, and the sub threshold current in the MOSFET channel have all been examined in order to better understand the device's electrical properties. The coulomb, phonon, and surface roughness scattering effects on charge carrier mobility in the MOSFET channel have all been examined. Finally, the influence of the Fin layer shape on the performance of the MOSFET was examined in this review.

Keywords: Electrical, bulk, threshold, mobility, layer, width, structure

Introduction

Introduction to the MOSFET technology

The challenges with planar or bulk Si-CMOS technology are becoming more prevalent as devices continue to shrink. As a result of these issues, the devices are no longer suitable for use in industry, such as VT roll off, drain-induced barrier lowering (DIBL), and a host of other short channel effects, such as increased leakage currents such as subthreshold S/D leakage and gate induced drain leakage (GIDL). Even if lowering the supply voltage Vdd, which reduces power consumption and the negative effects of heated carriers, has a marginal impact on performance. Lowering the VT may increase performance.

High-k gate dielectric is being sought by researchers in order to allow for the use of a thicker physical oxide while still maintaining acceptable channel control, although this has not yet been accomplished to the point of being useful. Other issues with Si include band alignment, thermal instability, and more. Researchers are now focusing their attention on metal gate electrodes due to the issue of thermal instability. To yet, however, no metal gates with appropriate job functions have been discovered. Due to random dopant fluctuations (at tiny gate lengths) and higher impurity dispersion (and hence lower mobility), polysilicon is still employed when this isn't possible. Shorter channel lengths increase off-state leakage current and standby power because it is more difficult to maintain the electrostatic integrity of devices – doping concentration in the channel must be increased and the source and drain junctions must become shallower – but these trends are offset by increased junction leakage and higher series resistances. The electrostatic integrity and, thus, the short channel immunity of fully depleted devices, particularly double gate devices, are greatly improved [2]. The MOSFET transistors, in addition to their outstanding channel control, give about double the on current compared to planar transistors. Dual gate MOSFETS, despite the fact that channel doping was not increased, were nonetheless more efficient. Because of this, a minimal gate leakage is achieved while also improving carrier mobility [3]. Double-gate MOSFETS may be used instead of planar MOSFETS in order to continue along the road of downsizing, as discussed in this article [1].

SOI and bulk MOSFETS

In the late 1990s and early 2000s, MOSFETS were often referred to as SOI MOSFETS produced on SOI wafers. Due of the difficulties associated with the short channel effect (SCE), the initial double-gate transistors were mostly shown on SOI substrates [4, 5, 6, 7-12]. SOI MOSFETS are MOSFETS constructed on SOI wafers. Due to the fact that no shallow trench isolation (STI) technique is needed and the source/drain regions have no leakage channel at the junction depth of the source/drain regions, these devices are noted for their ease of manufacturing and high scalability. The low parasitic capacitances of these SOI devices make them ideal for high-speed circuits.

Single- and double-gated floating body SOI devices may suffer from floating body issues [12] depending on their doping, Si film thickness, and bias conditions. The fault density and cost of SOI wafers are both greater than those of bulk-Si wafers. Since the thick buried oxide has poor heat transmission, the channel heat created by SOI FETs cannot be readily dispersed over the substrate. Instead of traditional four-terminal MOSFETS, the SOI MOSFET replaces them with three-terminal (body floating) devices, requiring active splitting [8] for narrow and depletion channels. Because of the three-terminal features, this reduces the operating range of the circuit. Because of this, four-terminal MOSFETS created by attaching the fin body directly to the Si substrate should be considered instead. They are known as "body-tied" MOSFETS or bulk MOSFETS [13] since they are fabricated on bulk-Si wafers. Because the body's cross-section resembles the Greek letter, when body-tied MOSFETS were initially disclosed, they were referred to as Omega MOSFETS. Because the gate structure resembles an, F.-L. Yang *et al*. referred to their MOSFET as an "omega FET" in their 2002 IEDM paper [8]. For this reason, we dubbed the body-tied MOSFET a "bulk MOSFET" in order to distinguish it from other MOSFETS such as the SOI and omega varieties. Figure 1, which depicts cross-sectional views of SOI and bulk MOSFETS with the chopped fin body, provides a simple explanation of MOSFET categorization.

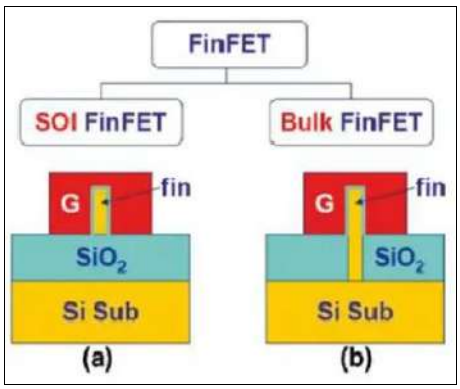

Fig 1: Classification of MOSFETS using structures [8]

There is a floating and a tethered fin body for the SOI and bulk MOSFETS. 'G' stands for 'gate electrode.' As contrast to three-terminal MOSFETS, bulk MOSFETS are more known to IC design engineers, and their fabrication methods are compatible with those of standard planar (or 2-D) channel CMOS devices manufactured on bulk-Si wafers. Figure 2 shows a schematic 3-D perspective of the bulk MOSFET. The width of the fin body (Wfin) and the height (Hfin) are shown here. The height of a fin is defined as the distance from the oxide isolation area to the top of the fin body. Device isolation is achieved by the thickness of the field oxide, which is measured in TFOX. xj denotes the depth of the source/drain junction, which is shown in the figure. Using the fin body, the substrate may be heated by heat emitted from the channel. As opposed to SOI MOSFETS, which suffer from high wafer costs, high defect densities, the floating body effect, and poor heat dissipation, bulk MOSFETS have better heat dissipation. They also have greater heat dissipation qualities than SOI MOSFETS, yet they retain approximately the same scalability [14].

Electrical Characteristics of MOSFET

Surface potentials at the source and drain end of a MOSFET are used to convey all of the device's features. Separate solutions for various operating zones are offered in the threshold voltage method.

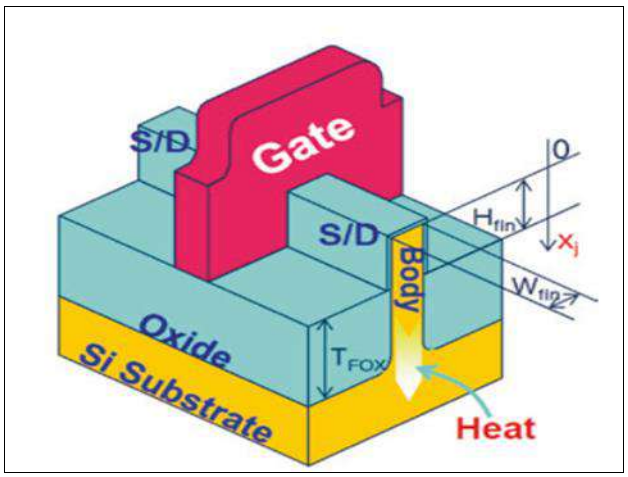

Fig 2: Three-dimensional schematic of bulk MOSFET. H_{fin} and W_{fin} represent fin height and width, respectively [8]

Linear Region

This is the region where vds climbs linearly with vds for a given vg > vt. As a first approximation in the linear region, Ids is given by [15].

vt is a measure of the oxide capacitance per unit area. The other three terms are W, L, and vt, which refer to the effective channel width, effective channel length, and the effective mobility of channel impurity atoms.

Indicator Region of Saturation

There are no further increases in this region. Again, a rough estimate of the saturation zone is [16].

It is the thickness of the depletion layer that determines Xd, whereas the thickness of the oxide does the same thing.

Exclusion Zone

When there is no channel between the source and drain, the drain current decomposes exponentially, resulting in subthreshold current. The low concentration of electrons in the channel makes the electric field in the channel weak, hence the diffusion of carriers is responsible for the subthreshold current. Subthreshold current [15] is an estimate.

Is the differential in work function between the gate electrode and the silicon body, which is nearly entirely intrinsic.

Figure 3 depicts the output characteristics of a MOSFET, while Figures 4 and 5 illustrate the transfer characteristics of the same device. According to Fig. 3, MOSFETS with channel length of 10 nm, Fin layer thickness of 30nm, and gate voltages as high as 5 V have output characteristics that are shown in the figure. Experimental data is represented as symbols, while simulation results are shown as solid lines [17].

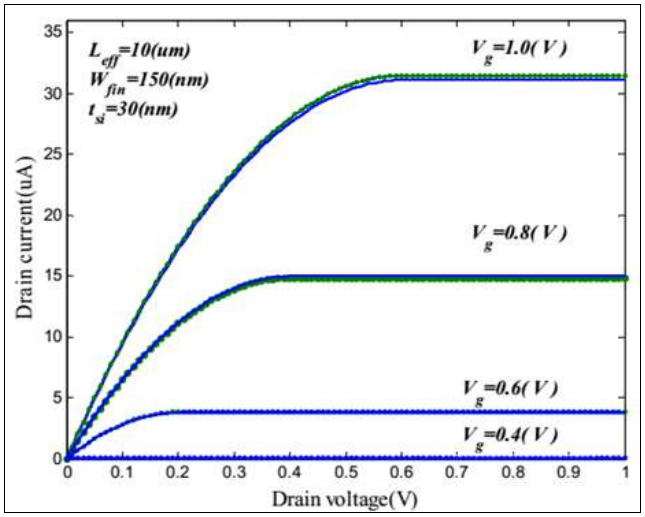

Fig 3: Output characteristics of MOSFET [17]

Figure 5 shows the n-Channel MOSFET subthreshold current [17] is the threshold voltage for MOSFET:

$$V_{th} = \phi + n\frac{kT}{q}\ln\left(\frac{2C_{ox}kT}{q^2 n_i t_{si}}\right) + \frac{h^2\pi^2}{2m_{ds}W_{si}^2}$$

Effective mobility of Charge Carriers in MOSFET

The applied Effective electric field, is defined as [18]

$$E_{eff} = \frac{1}{2}\frac{q}{\varepsilon}\left(\frac{N_{inv}}{2} + N_{sub}\times t_{si}\right) \quad \text{----------(E)}$$

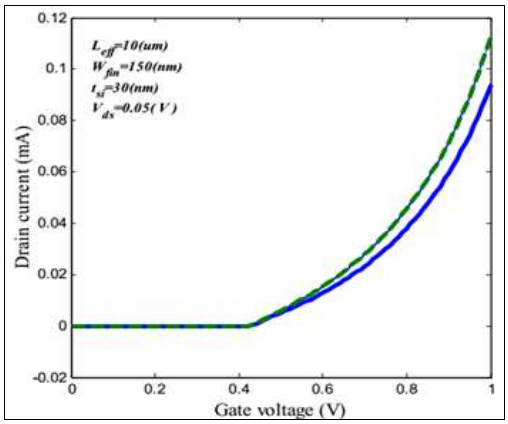

Fig 4: Transfer Characteristics of FinFT [17]

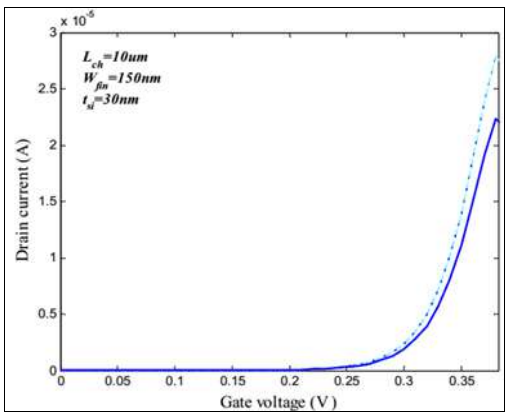

Fig 5: Subthreshold current of n-Channel MOSFET [17]

Numerous scattering processes exchange momentum with the semiconductor to stabilise mobility. Crystallographic flaws, such as atomic ionisation and surface roughness as well as interface trapped charges, are all responsible for the scattering. Many studies have focused on the inversion channel's mobility [19].

The effective mobility of the MOSFET is determined by a combination of three mechanisms:

1. Scattering by Coulomb [20], which may be represented mathematically by the equation below?

$$\mu_{col} = \mu_0^{ph}\left(1 + \frac{E_{eff}}{E_c^{col}}\right)^{v^{col}}$$

2. This equation is used to describe the dispersion of phonons [20]:

$$\mu_{ph} = \frac{\mu_0^{ph}}{\left(1+\frac{E_{eff}}{E_c^{ph}}\right)^{v^{ph}}}$$

3. Surface roughness scattering [21], given by the following equation:

$$\mu_{sr} = \mu_0^{sr}\left(\frac{E_{eff}}{E_{effo}}\right)^{\gamma}$$

These three factors that contribute to the total mobility can be combined using Matthiesen's rule [18], which states that

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{col}} + \frac{1}{\mu_{sr}} \quad \text{----------(F)}$$

Mobility is influenced by a number of different variables, all of which may be found on the right side of the letter (F) (F). Effective electric field is shown in the figure as influencing inversion layer mobility.

The right-side components in Equation (F) indicate eff, a measure of total mobility (F) mobility-related phenomena. The graphic shows that the inversion layer's mobility is affected by the effective electric field.

In this section, we examine the effect of fin shape on the performance of MOSFETS.

Many years of miniaturisation in the electronics sector may be attributed to scaling MOSFETS [22]. To date, it has made a substantial contribution to semiconductor industry growth by providing the pivot for its hitherto unimaginable growth. Smaller-featured devices have a higher risk of introducing SCEs, such as Vth roll-off, hot carrier effects, drain induced barrier lowering (DIBL), and enhanced subthreshold swing and leakage currents. Since Moore's predictions couldn't be kept up with, the industry has come to a halt with bulk devices. Because of the high power consumption and manufacturing variability, conventional transistors could not be scaled down to 22nm. Innovative materials and non-classical device designs must be used to improve performance in order to overcome these problems. MOSFET transistors surpass MOS transistors in terms of short channel effects (SCE) [23]. By using MOSFETS, which have no space overhead and do not need an additional mask,

low leakage multi-threshold circuits are conceivable. MOSFETS have a few downsides, such as an increased leakage current caused by undesirable side effects such as corner effects, quantum effects, and tunnelling, for example. The charge sharing effect is responsible for the early corner inversion in Trigate MOSFET. This phenomenon is described in [23, 25], which leads to the development of channels with varying threshold voltages in response to this event. For small devices, the density of the trigate MOSFET corner is comparable to that of the planar surface channel region, which has a higher density of mobile carriers. The bulk of the device's electricity is sent to the gadget's corners, which are responsible for turning it on. On-state current increases as channel widths shrink, and the electron density distributions in the corners are higher than those elsewhere. It really has a detrimental effect on productivity. It's a MOSFET with rounded edges, the PC-MOSFET In order to increase on- and off-state performance for the same channel length, it is possible to change the shape of the fin from a round to a tapered one.

It has been demonstrated in Figure 6 and Figure 7 that a 3D device design for Trapezium PC MOSFET, where Wtop is believed to be 1nm and Wbottom is considered to be 15nm, is possible. Wtop is considered to be 5nm, while Wbottom is considered to be 1nm [28].

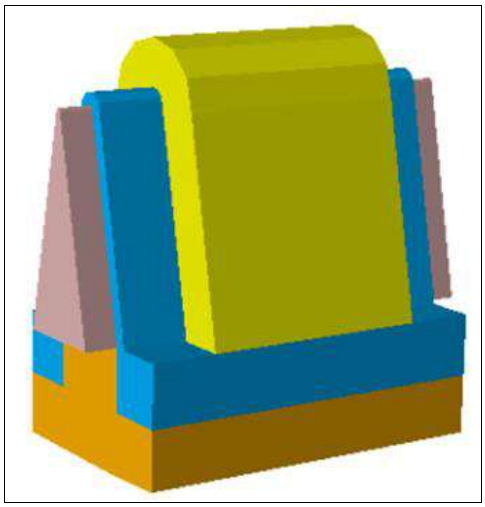

Fig 6: Trapezium PC MOSFET device structure with Wtop=1nm and Wbottom=15nm [28]

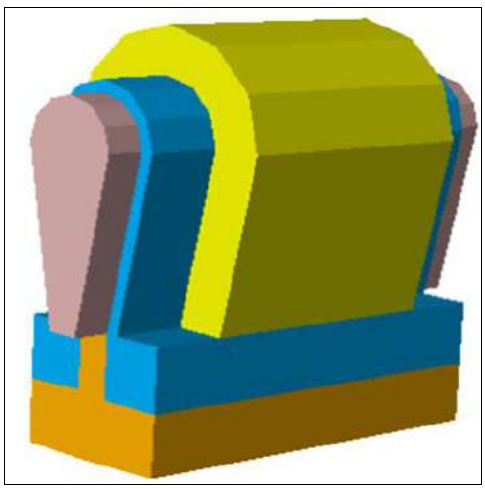

Fig 7: Inverse trapezium PC MOSFET device structure with Wtop=15nm and Wbottom=5nm [28]

Tz MOSFET VS Wtop and inverse Tz MOSFET VS Wtop threshold voltage simulation curves are illustrated in Figures 8 and 9.

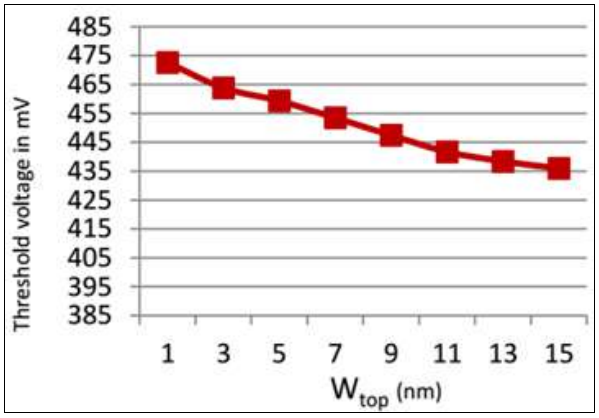

Fig 8: Threshold voltage characteristics of Tz PC MOSFET with varying W_{top} [28]

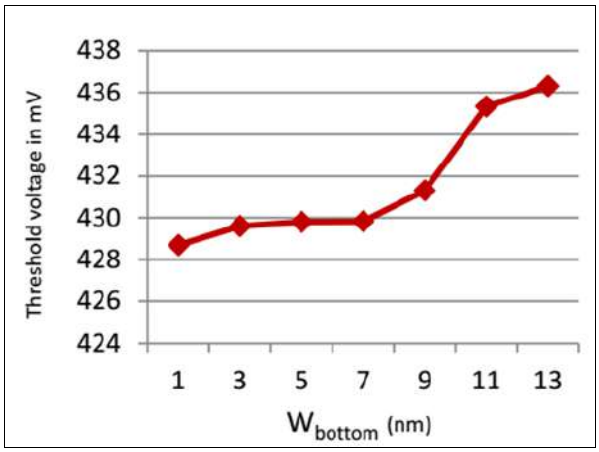

Fig 9: Threshold voltage characteristics of inverse Tz PC MOSFET with varying W_{top} [28]

Conclusion

Various MOSFET structures have been analysed, as well as the three-dimensional bulk MOSFET structure. An investigation on the MOSFET's electrical properties has been completed. The characteristic curves for output current-voltage, transfer characteristics, and subthreshold current in n channel MOSFETS were studied. Consideration has been given to how scattering affects the mobility of charge carriers in the MOSFET channel. In this research, the thresholf voltage characteristics of trapizoidal PC MOSFET with varied top Fin layer width were evaluated, as was the impact of Fin layer shape on MOSFET performance. MOSFET's efficient electrical and mechanical qualities may be predicted using these features.

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